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EXAMINER	
ZHONG, CHAD	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/817,008	Applicant(s) PEKKALA ET AL.	
	Examiner Chad Zhong	Art Unit 2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-79 are presented for examination.

2. It is noted that although the present application does contain line numbers in specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the Examiner and Applicant all future correspondence should include the recommended line numbering.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Further, the spelling on the title is incorrect as stated, appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-28 and 30-79 are rejected under 35 U.S.C. 102(e) as being anticipated by Beukema et al. (hereinafter Beukema), US 2002/0073257.

6. As per claim 1, Beukema teaches an integrated circuit functioning as an InfiniBand channel adapter and an InfiniBand switch, comprising:

a plurality of InfiniBand media access controllers (MACs), for transceiving InfiniBand packets (Fig 1);

a plurality of local bus interfaces, for performing addressed data transfers on a plurality of local buses coupled thereto (Fig 1; pg 1, [0005]);

a bus router, for performing transport layer operations between said plurality of InfiniBand MACs and said plurality of local bus interfaces (pg 2, [0020], [0024]); and

a transaction switch, coupled to each of said plurality of InfiniBand MACs, said plurality of local bus interfaces, and said bus router, for switching data and transactions therebetween (pg 8, [0082]; Fig 1).

7. As per claim 2, Beukema teaches the integrated circuit of claim 1, further comprising:

a plurality of transaction queues, associated with said plurality of InfiniBand MACs, said plurality of local bus interfaces, and said bus router, coupled to said transaction switch, for storing said transactions (pg 4, [0039-0041], [0043]).

8. As per claim 3, Beukema teaches the integrated circuit of claim 1, further comprising:

a memory, shared by said plurality of InfiniBand MACs, said plurality of local bus interfaces, and said bus router, for buffering data received thereby (pg 4, [0039]-[0041], [0043]).

9. As per claim 4, Beukema teaches the integrated circuit of claim 3, wherein said transaction switch comprises:

a buffer manager, for allocating portions of said memory to said plurality of InfiniBand MACs, said plurality of local bus interfaces, and said bus router, for buffering said data received thereby (pg 4, [0039-0041], [0043]).

10. As per claim 5, Beukema teaches the integrated circuit of claim 4, wherein said buffer manager performs said allocating in a substantially as-needed manner (pg 4, [0039-0041]; [0043]).

11. As per claim 6, Beukema teaches the integrated circuit of claim 3, wherein said bus router is configured to write an InfiniBand packet header into said memory via said transaction switch along

addressed data stored in said memory by one of said plurality of local bus interfaces to create an InfiniBand packet (pg 3, [0034]).

12. As per claim 7, Beukema teaches the integrated circuit of claim 3, wherein said plurality of local bus interfaces are configured to read a payload portion of an InfiniBand packet stored in said memory and to transmit said payload portion on one or more of the plurality of local buses coupled thereto (pg 5, [0059]).

13. As per claim 8, Beukema teaches the integrated circuit of claim 7, wherein said payload portion is located in said memory at an offset specified in a transaction posted by said bus router to said plurality of local bus interfaces via said transaction switch (p 5, [0059]; pg 7, [0077]; Fig 1).

14. As per claim 9, Beukema teaches the integrated circuit of claim 1, wherein at least one of said plurality of local bus interfaces comprises a PCI bus interface (pg 7, [0075]).

15. As per claim 10, Beukema teaches the integrated circuit of claim 1, wherein said transaction switch is configured to receive a transaction posted by a first of said plurality of InfiniBand MACs in response to a packet received by said first of said plurality of InfiniBand MACs and to selectively switch said transaction to one of a second of said plurality of InfiniBand MACs and said bus router (pg 8, [0082]; pg 1, [0007]).

16. As per claim 11, Beukema teaches the integrated circuit of claim 10, wherein said transaction switch selectively switches said transaction based on an InfiniBand destination local identification value included in said transaction (pg 1, [0007]; pg 8, [0082]).

17. As per claim 12, Beukema teaches the integrated circuit of claim 11, wherein said transaction switch selectively switches said transaction to said bus router if an entry associated with said InfiniBand

destination local identification value in a mapping table of said transaction switch indicates said transaction is destined for said bus router (pg 8, [0082], [0084]; pg 7, [0077]).

18. As per claim 13, Beukema teaches the integrated circuit of claim 12, wherein said transaction switch selectively switches said transaction to one of said plurality of InfiniBand MACs based on which of said plurality of InfiniBand MACs is associated with said InfiniBand destination local identification value in said mapping table if said entry indicates said transaction is not destined for said bus router (pg 8, [0082], [0084]; pg 7, [0077]).

19. As per claim 14, Beukema teaches the integrated circuit of claim 11, wherein said first MAC parses said InfiniBand destination local identification value from said packet (pg 5, [0059]).

20. As per claim 15, Beukema teaches the integrated circuit of claim 10, wherein said transaction includes an InfiniBand virtual lane number parsed from said packet (pg 4, [0042], [0039]).

21. As per claim 16, Beukema teaches the integrated circuit of claim 10, wherein said transaction includes a destination queue pair number parsed from said packet (pg 4, [0039]).

22. As per claim 17, Beukema teaches the integrated circuit of claim 1, wherein said transaction switch is configured to receive a transaction posted by said bus router and to selectively switch said transaction to one of said plurality of InfiniBand MACs and one of one of said plurality of local bus interfaces (pg 8, [0082]).

23. As per claim 18, Beukema teaches the integrated circuit of claim 17, wherein said transaction switch selectively switches said transaction based on a transaction type value included in said transaction (pg 8, [0082], [0084]).

24. As per claim 19, Beukema teaches the integrated circuit of claim 18, wherein said transaction switch selectively switches said transaction to one of said plurality of local bus interfaces based on whether a local bus address included in said transaction falls into one or more predetermined address ranges of the plurality of local buses (pg 8, [0082]; pg 7, [0077]).

25. As per claim 20, Beukema teaches the integrated circuit of claim 17, wherein said transaction includes an address in an address range of the plurality of local buses (pg 7, [0077]).

26. As per claim 21, Beukema teaches the integrated circuit of claim 1, further comprising a local bus bridge coupled between said plurality of local bus interfaces for buffering data therebetween (pg 4, [0039]-[0041]).

27. As per claim 22, Beukema teaches the integrated circuit of claim 1, wherein said transaction switch is configured to receive a transaction posted by a first of said plurality of local bus interfaces in response to an addressed data transfer received by said first of said plurality of local bus interfaces and to switch said transaction to a second of said plurality of local bus interfaces (pg 8, [0082]).

28. As per claim 23, Beukema teaches a transaction switch for switching data between a plurality of data devices, comprising:

a memory, shared by the plurality of data devices for buffering data received thereby (pg 4, [0039-0041]);

multiplexing logic, for controlling the transfer of data between the plurality of data devices and said memory (pg 8, [0082]); and

control logic, for controlling said multiplexing logic; wherein the plurality of data devices comprise a plurality of packetized data devices and a plurality of addressed data devices (pg 8, [0082]; pg 1, [0007]);

wherein said control logic is configured to selectively control said multiplexing logic to transfer data

through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices (pg 8, [0082], [0084]).

29. As per claim 24, Beukema teaches the transaction switch of claim 23, wherein said control logic is further configured to selectively control said multiplexing logic to transfer data through said memory between two of said addressed data devices (pg 8, [0082], [0084]).

30. As per claim 25, Beukema teaches the transaction switch of claim 23, wherein said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices concurrently (pg 8, [0082], [0084]).

31. As per claim 26, Beukema teaches the transaction switch of claim 23, wherein at least two of said packetized data devices comprise InfiniBand interfaces (pg 7, [0075]).

32. As per claim 27, Beukema teaches the transaction switch of claim 23, wherein at least two of said addressed data devices comprise PCI bus interfaces (pg 7, [0076]).

33. As per claim 28, Beukema teaches the transaction switch of claim 23, further comprising:

a buffer manager, for allocating portions of said memory to the plurality of data devices for buffering said data (pg 4, [0039-0041], [0043]).

34. As per claim 30, Beukema teaches the transaction switch of claim 23, wherein said control logic is configured to selectively control said multiplexing logic to transfer data through said memory between two of said packetized data devices and between one of said packetized data devices and one of said addressed data devices in response to a transaction posted to the transaction switch by the plurality of data devices (pg 8, [0082], [0084]).

35. As per claim 31, Beukema teaches the transaction switch of claim 30, wherein said transaction comprises a command to transfer data between said memory and one of the plurality of data devices (pg 8, [0082], [0084]).

36. As per claim 32, Beukema teaches the transaction switch of claim 31, wherein said transaction comprises an address of a buffer within said memory wherein is stored said data to be transferred in response to said command (pg 7, [0077]; pg 5, [0059]; pg 4, [0039]).

37. As per claim 33, Beukema teaches the transaction switch of claim 32, wherein said transaction comprises an offset within said buffer for addressing portions of said data (pg 4, [0047]; pg 7, [0077]).

38. As per claim 34, Beukema teaches the transaction switch of claim 30, wherein said transaction comprises a tag for uniquely identifying said transaction from other transactions posted to the transaction switch by the plurality of data devices (pg 7, [0077]).

39. As per claim 35, Beukema teaches the transaction switch of claim 23, wherein the plurality of data devices comprise a transport layer device, wherein the transaction switch is configured to receive transactions from said transport layer device for performing protocol translation of data between said one of said packetized data devices and said one of said addressed data devices (pg 2, [0020], [0023]; pg 1, [0007]).

40. As per claim 36, Beukema teaches a transaction switch for switching transactions and data between a plurality of data interfaces, the transaction switch comprising:

a memory, shared by the plurality of data interfaces, for buffering data received thereby;

a plurality of transaction queues, associated with each of the plurality of data interfaces, configured to store transactions, said transactions adapted to convey information to enable the plurality of data interfaces to transfer said data according to a plurality of disparate data transfer protocols supported

thereby (pg 1, [0007]; pg 4, [0039]-[0041]); and

control logic, configured to route said data through said shared memory between the plurality of data interfaces and to switch said transactions between the plurality of data interfaces (pg 8, [0082]).

41. As per claim 37, Beukema teaches the transaction switch of claim 36, wherein said control logic is configured to route said data between the plurality of data interfaces through said shared memory in response to said transactions received from said plurality of transaction queues (pg 8, [0082], [0084]; pg 7, [0039-0041]).

42. As per claim 38, Beukema teaches the transaction switch of claim 36, wherein at least a portion of said plurality of transaction queues is configured to store transactions adapted to convey information necessary to transfer data according to an InfiniBand protocol (pg 4, [0039-0041]; pg 7, [0075]).

43. As per claim 39, Beukema teaches the transaction switch of claim 36, wherein at least a portion of said plurality of transaction queues is configured to store transactions adapted to convey information necessary to transfer data according to an PCI bus protocol (pg 7, [0076]).

44. As per claim 40, Beukema teaches the transaction switch of claim 36, wherein said control logic is further configured to modify a transaction received from one of said plurality of transaction queues associated with a first of the plurality of data devices and to send said modified transaction to another one of said plurality of transaction queues (pg 1, [0007]).

45. As per claim 41, Beukema teaches an integrated circuit, comprising:

at least three data interfaces;

a memory, shared by said at least three data interfaces for buffering data therebetween (pg 4, [0039]); and

a transaction switch, coupled to said at least three data interfaces and said memory, for dynamically allocating portions of said memory to said at least three data interfaces for storing data therein, and for controlling access to said allocated portions of said memory by each of said at least three data interfaces (pg 8, [0082]);

wherein at least one of said at least three data interfaces is of a different type than the others (Fig 1; pg 1, [0007]).

46. As per claim 42, Beukema teaches the integrated circuit of claim 41, wherein at least one of said at least three data interfaces is a packetized data interface and at least one of said at least three data interfaces is an addressed data interface (pg 1, [0007]; pg 3, [0034]).

47. As per claim 43, Beukema teaches the integrated circuit of claim 42, wherein said at least one packetized data interface is an InfiniBand interface (pg 7, [0075]).

48. As per claim 44, Beukema teaches the integrated circuit of claim 42, wherein said at least one addressed data interface is a PCI interface (pg 7, [0075]).

49. As per claim 45, Beukema teaches the integrated circuit of claim 41, wherein said transaction switch is configured to receive a transaction from a first of said at least three data interfaces and to selectively switch said transaction to one of another of said at least three data interfaces (Fig 1; pg 8, [0082]).

50. As per claim 46, Beukema teaches the integrated circuit of claim 45, wherein said transaction is a packetized data transaction including packet destination information (pg 1, [0007]).

51. As per claim 47, Beukema teaches the integrated circuit of claim 46, wherein said transaction switch is configured to selectively switch said packetized data transaction to said another of said at least

three data interfaces based on said packet destination information and information stored in a mapping table of said transaction switch (pg 7, [0076]; pg 8, [0082], [0084]).

52. As per claim 48, Beukema teaches the integrated circuit of claim 47, wherein said transaction switch is configured to selectively switch said packetized data transaction to said another of said at least three data interfaces further based on information stored in a table mapping said packet destination information to said at least three data interfaces (pg 7, [0076]; pg 8, [0082], [0084]).

53. As per claim 49, Beukema teaches the integrated circuit of claim 45, wherein in a first instance of said transaction said first and one of another of said at least three data interfaces are of a same type of interface, wherein in a second instance of said transaction said first and one of another of said at least three data interfaces are of a different type of interface (Fig 1).

54. As per claim 50, Beukema teaches the integrated circuit of claim 49, wherein in said first instance each of said first and one of another of said at least three data interfaces is a packetized data interface type (pg 1, [0007]).

55. As per claim 51, Beukema teaches the integrated circuit of claim 49, wherein in said second instance said first of said at least three data interfaces is a packetized data interface type and said one of another of said at least three data interfaces is an interface type capable of translating between packetized and addressed data (pg 1, [0007]).

56. As per claim 52, Beukema teaches the integrated circuit of claim 49, wherein in said second instance said first of said at least three data interfaces is a packetized data interface type and said one of another of said at least three data interfaces is a transport level data interface (Fig 1; pg 1, [0007]).

57. As per claim 53, Beukema teaches the integrated circuit of claim 45, wherein said transaction

switch is configured to modify said transaction received from said first of said at least three data interfaces prior to selectively switching said received transaction to said one of another of said at least three data interfaces (pg 1, [0007]).

58. As per claim 54, Beukema teaches the integrated circuit of claim 41, wherein said transaction switch is configured to receive a transaction from a first of said at least three data interfaces and to selectively switch said received transaction to two or more of another of said at least three data interfaces (pg 1, [0007]; pg 8, [0082]).

59. As per claim 55, Beukema teaches the integrated circuit of claim 41, further comprising:

a plurality of transaction queues, coupled between said transaction switch and said at least three data interfaces, for storing transactions between said transaction switch and said at least three data interfaces (pg 4, [0039-0041]).

60. As per claim 56, Beukema teaches the integrated circuit of claim 55, further comprising a programmable register for specifying for at least a plurality of said plurality of transaction queues a number of transaction slots to be allocated for storing said transactions (pg 4, [0039-0041]).

60. As per claim 57, Beukema teaches the integrated circuit of claim 41, wherein at least one of said at least three data interfaces comprises a bus router for performing a transport layer function between at least two other of said at least three data interfaces which support disparate data protocols (pg 1, [0007]; pg 8, [0082]).

61. As per claim 58, Beukema teaches the integrated circuit of claim 41, further comprising: a bus router, coupled to the transaction switch, for performing transport layer functions between said at least three data interfaces having different data protocols (pg 1, [0007]; pg 8, [0082]).

62. As per claim 59, Beukema teaches the integrated circuit of claim 58, wherein said bus router is configured to write packet header information into said allocated portions of said memory (pg 1, [0007]; pg 4, [0039]).

63. As per claim 60, Beukema teaches the integrated circuit of claim 41, wherein a first of said at least three data interfaces is configured to post a transaction to said transaction switch for instructing a second of said at least three data interfaces to transfer data to or from an offset in one of said allocated portions of said memory associated with a payload portion of a data packet (pg 7, [0077]; pg 8, [0082]; pg 5, [0059]).

64. As per claim 61, Beukema teaches the integrated circuit of claim 41, wherein said transaction switch is further configured to de-allocate said portions of said memory (pg 5, [0050-0051]; pg 4, [0045-0046]).

65. As per claim 62, Beukema teaches the integrated circuit of claim 41, wherein said transaction switch is configured to dynamically allocate said portions of said memory to said at least three data interfaces on a substantially as needed basis (pg 4, [0039-0041]; pg 5, [0050-0051]).

66. As per claim 63, claim 63 is rejected for the same reasons as rejection to claim 1 above.

67. As per claim 64, claim 64 is rejected for the same reasons as rejection to claim 1 above.

68. As per claim 65, Beukema teaches the integrated circuit of claim 64, wherein said transaction switch is further configured to switch an addressed data transaction from said routing device to said second of said plurality of addressed data interfaces (pg 8, [0082]).

69. As per claim 66, Beukema teaches the integrated circuit of claim 63, wherein each of said plurality of packetized data interfaces comprises a packetized interface selected from a list comprising an

Ethernet interface, a FibreChannel interface, an IEEE 1394 interface, a SONET interface, an ATM interface, a SCSI interface, a serial ATA interface, an OC-48 interface, and an OC-192 interface (pg 3, [0032]).

70. As per claim 67, claim 67 is rejected for the same reasons as rejection to combination of claims 1 and 2 above.

71. As per claim 68, Beukema teaches the InfiniBand hybrid channel adapter/switch of claim 67, wherein at least a subset of said plurality of transaction queues comprise an input queue for said plurality of InfiniBand ports to post said transaction to said switch (pg 4, [0039-0041]; pg 2, [0024]).

72. As per claim 69, Beukema teaches the InfiniBand hybrid channel adapter/switch of claim 67, wherein said plurality of transaction queues comprise an output queue for said transaction switch to send said transaction to said plurality of InfiniBand ports and said at least one addressed data bus interface (pg 4, [0039-0041]).

73. As per claim 70, Beukema teaches the InfiniBand hybrid channel adapter/switch of claim 67, wherein said at least one addressed data bus interface is coupled to a data bus selected from a list comprising a Rapid I/o bus, a VESA bus, an ISA bus, a PCI bus, an LDT bus, an SDRAM bus, a DDR SDRAM bus, and a RAMBUS (pg 3, [0034]).

74. As per claim 71, claim 71 is rejected for the same reasons as rejection to claim 1 above.

75. As per claim 72, Beukema teaches the method of claim 71, wherein each of said switching steps is performed substantially concurrently (pg 3, [0030]).

76. As per claim 73, Beukema teaches the method of claim 71, wherein said packetized data

transaction comprises a transaction associated with an InfiniBand packet transmission (pg 7, [0075]).

77. As per claim 74, Beukema teaches the method of claim 71, wherein said addressed data transaction comprises a transaction associated with a PCI bus data transfer (pg 7, [0076]).

78. As per claim 75, Beukema teaches The method of claim 71, further comprising:

switching a packetized data transaction from one of the plurality of packetized data devices to the routing device (pg 8, [0082]).

79. As per claim 76, Beukema teaches The method of claim 71, further comprising:

switching an addressed data transaction from the routing device to one of the plurality of addressed data devices; and

switching a packetized data transaction from the routing device to one of the plurality of packetized data devices (pg 8, [0082], [0084]).

80. As per claim 77, Beukema teaches the method of claim 71, further comprising: performing protocol translation in a transfer of data between the packetized data interface and the addressed data interface without double-buffering the data (pg 1, [0007]).

81. As per claim 78, Beukema teaches the method of claim 71, further comprising: parsing a packet and generating said packetized data transaction prior to said switching said packetized data transaction (pg 1, [0007]).

82. As per claim 79, Beukema teaches a transaction switch in a network device having a buffer memory and plurality of data devices, including packetized and addressed data devices, the transaction switch comprising:

a buffer manager, for allocating portions of the buffer memory to the plurality of data devices on an

as-needed basis (pg 4, [0039]);

a plurality of data paths, for providing the plurality of data devices access to the buffer memory (Fig 1);

a mapping table, for storing packet destination identification information (pg 7, [0077]);

a plurality of transaction queues, for transferring transactions between the transaction switch and the plurality of data devices (pg 4, [0039-0041]); and

control logic, for selectively switching data between the plurality of data devices based on said mapping table information and in response to said transactions (pg 7, [0077]; pg 8, [0082], [0084]).

Claim Rejections - 35 USC § 103

83. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

84. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beukema et al. (hereinafter Beukema), US 2002/0073257, in view of 'Official Notice'.

85. As per claim 29, Beukema does not explicitly teaches the transaction switch of claim 28, wherein said buffer manager is configured to perform said allocating on substantially a first-come-first-serve basis. "Official Notice" is taken that the concept and advantages of providing for FIFO queue is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include FIFO with Beukema because it would provide for fair queuing, by allowing flows that arrive first get processed and allocated first will improve the efficiency of system.

Conclusion

86. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Apparatus And Method For Disparate Fabric Data And Transaction Buffering Within Infiniband Devices".

i. US 6535518 Hu et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chad Zhong whose telephone number is (703) 305-0718. The examiner can normally be reached on M-F 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on 703-305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

CZ
June 29, 2004

ZARNI MAUNG
PRIMARY EXAMINER